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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

PRH

PRG

Office Action Summary	Application No. 09/423,415	Applicant(s) MORIAKA
	Examiner Anthony Blackman	Art Unit 2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *THREE* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 28, 2002* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *11-20 and 22-34* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *11-20 and 22-34* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The following title is suggested: Image Processing Wherein Decompression and Compression Methods Provide Faster Transmission Of Texture Data Between A Texture Buffer And Storage Device To/From a Storage Device.

Claim Objections

3. Claim 23 is objected to because of the following informalities: there is no period after "said processor" of line 7. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14-15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over FURUHASHI et al US Patent Number 6,011,564 in view of DYE US Patent number 5,664,162.

6. Consider claims 14-15 and 23. FURUHASHI et al disclose the means of an apparatus for processing (Abstract, lines 1-2), comprising: a processor including a data decompression/decoding circuit (column 3, lines 33-56, and column 4, lines 51-61); a first storage device having texture data and electronically coupled to said processor (figure 5, elements 42-43), reading said compressed data (figure 5, elements 54-55), however, does not disclose; a first data bus and a second data bus, a first data bus and a second data bus, wherein said first data bus carries texture data between said texture buffer and said processor faster than said second data bus carries texture data from said storage device and said processor, storing said decompressed texture data in a texture buffer, a texture buffer having decompressed texture data and electronically coupled to said processor; wherein transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor. DYE disclose the aforementioned features; a first data bus and a second data bus (figure 1, elements 102 and 118), DYE provides the suggestion wherein said first data bus carries texture data between said texture buffer and said processor faster than said second data bus carries texture data from said storage device and said processor (column 2, lines 53-54, column 3, lines 17-23, column 15, lines 23-62, column 17, line 42 to column 18 line 6, and column 19, lines 1-9), storing said decompressed texture data in a texture buffer (column 2, lines 53-54, column 3, lines 17-23, column 15, lines 23-62, column 17, line 42 to column 18 line 6, and column 19, lines 1-9), a texture buffer having decompressed texture data and electronically coupled to said processor (column 2, lines 53-54, column 3, lines 17-23, column 15, lines 23-62,

column 17, line 42 to column 18 line 6, and column 19, lines 1-9); wherein transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor ((column 2, lines 53-54, column 3, lines 17-23, column 15, lines 23-62, column 17, line 42 to column 18 line 6, and column 19, lines 1-9). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the graphics accelerator means of DYE because both inventions share similar technological environments of decompression/decoding and compression/coding graphics imaging data. Further, the addition of Dye "...provides a graphics processor to perform high level graphics functions and to achieve faster graphic transfer..." (Column 3, lines 18-24).

7. Claims 11-13, 16-20, 22, 24, 26-28, 30-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over FURUHASHI et al US Patent Number 6,011,564 in view of DYE US Patent Number 5,664,162, and further in view of TROELLER et al US Patent Number.

8. Consider claim 11. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROELLER et al disclose a frame buffer, wherein said processor stores image in said frame buffer. Therefore, it would have been obvious to a skilled artisan to modify the image processing system of FURUHASHI et al as modified by the data compression and decompression of digital information in a real-time environment (column 1, lines 5-10) because TROELLER et al "...provides processing power to manipulate billions of arithmetic operations per second across a wide-range of real world

applications so that the image data may be manipulated before it is compressed and stored (or transmitted over a network) or decompressed and displayed"(column 3, lines 8-14).

9. Consider claim 12. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROELLER et al disclose including the further comprising of a frame buffer, wherein said processor stores image data in said frame buffer (figure 2). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] a Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

10. Consider claim 13. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data (figure 1, elements 102 and 112, and figure 2, element 112). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

11. Consider claim 16. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose

wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data, and said processor stores said decompressed texture data in said texture buffer (figure 1, elements 102 and 112, and figure , element 112). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

12. Consider claim 17. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said data decompression circuit receives said read compressed texture data from said

FIFO storage device (figure 3, column 8, line 21 to column 9, line 6). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

13. Consider claim 18. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decompressed texture data (column 5, line 62 to column 6, line 30, and column 10, lines 52-57). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by

the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

14. Consider claim 20. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said texture data in said first storage device is compressed (figure 2). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing

common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

15. Consider claim 22. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose further comprising the step of converting said decompressed texture data to image data, and storing said image data in a frame buffer (FIGURES 1-2). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further,

TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

16. Consider claim 24. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose further comprising the step of performing palette conversion of said decompressed texture data prior to said step of storing said texture data (column 5, line 62 to column 6, line 30, and column 10, lines 52-57. Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the

workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

17. Consider claim 26. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said step of storing said decompressed texture data includes the step of updating said decompressed texture buffer with new decompressed data (figures 1-2). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

18. Consider claim 27. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said processor stores image data in said frame buffer (figures 1-2). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

19. Consider claim 28. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said step of storing said decompressed texture data includes the step of updating said decompressed texture buffer with new decompressed data (figures 1-2). Therefore it would have

been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

20. Consider claim 29. FURUHASHI et al as modified meet limitations for claims 14-15 and 23, however, does not expressly teach the aforementioned claim. TROLLER et al disclose wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data (figure 1, elements 102 and 112, and figure 2, element 112). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a

Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

21. Consider claim 30. FURUHASHI et al as modified meet limitations for claim 15, however, does not expressly teach the aforementioned claim. TROLLER et al provides the suggestion wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data (figure 3, column 8, line 21 to column 9, line 6). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing

common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

22. Consider claim 31. FURUHASHI et al as modified meet limitations for claim 30. TROLLER et al disclose limitations for claim 30, wherein said data compression circuit receives said read compressed texture data from said FIFO storage device (figure 3, column 8, line 21 to column 9, line 6). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al,

"...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

23. Consider claim 32. FURUHASHI et al as modified meet limitations for claim 29. TROLLER et al provides the suggestion disclosing limitations for claim 32 wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decompressed texture data (figure 2, elements 200 and 202, column 5, line 62 to column 6, line 53). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or

photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

24. Consider claim 34. FURUHASHI et al as modified meet limitations for claim 15. TROLLER et al disclose limitations for claim 34, wherein said texture data in said first storage device is compressed (figure 2). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the image processing system of FURUHASHI et al by the invention manipulating video and image data in system memory with a Video, imaging and compression (VIC) engine that consists of a DMA (direct memory access) controller to move data to and from system memory to the VIC engine...[including] I Bitstream processor optimized to perform variable bit length processing common in compression and de-compression algorithms"(column 3, lines 40-49) of TROLLER et al because both inventions, FURUHASHI et al as modified and TROLLER et al share similar functions regarding the compression and decompression or encoding and decoding systems geared to processing image data. Further, TROLLER et al, "...provides a system that permits the manipulation of video and image data rather than just displaying image data in a manner that merely emulates a television or photographs. The present invention frees up the workstation to sort or manipulate image data, to perform content recognition, as well as to compress or decompress the image data in real-time (column 4, lines 28-34)".

25. Claims 19, 25, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over FURUHASHI et al US Patent Number 6,011,564 in view of DYE US Patent number 5,664,162, and further in view of TROLLER et al US Patent Number 5,768,445, and still further in view of SCHILLING et al US Patent Number 6,236,405.

26. Consider claim 19. The modified FURUHASHI has wherein said processor includes a mip map generation circuit, and mip map generation circuit generating a mip map of said decompressed data. SCHILLING et al disclose the means of the above limitation (figure 8, element 816, column 8, lines 26-43). Therefore, it would have been obvious to a skilled artisan at the time of the invention to modify the image processing system of FURUHASHI et al by the texture mip mapping teaching of SCHILLING et al because both inventions share similar functions of texture mapping. Further, SCHILLING et al provides the following advantage - "..the present invention provides a data compression system to reduce memory storage and bandwidth requirements in a simple, yet fast manner, and to therefore reduce system costs" (column 2, lines 18-22).

27. Consider claim 25. The modified FURUHASHI further comprising the step of generating a mip map of said compressed texture data prior to said step of storing said decompressed texture data. SCHILLING et al disclose the above feature (figure 8, element 816, column 8, lines 26-43). Therefore, it would have been obvious to a skilled artisan at the time of the invention to modify the image processing system of FURUHASHI et al by the texture mip mapping teaching of SCHILLING et al because both inventions share similar functions of texture mapping. Further,

SCHILLING et al provides the following advantage - "..the present invention provides a data compression system to reduce memory storage and bandwidth requirements in a simple, yet fast manner, and to therefore reduce system costs" (column 2, lines 18-22).

28. Consider claim 33. The modified FURUHASHI has wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed texture data. SCHILLING et al disclose the above feature (figure 8, element 816, column 8, lines 26-43). Therefore, it would have been obvious to a skilled artisan at the time of the invention to modify the image processing system of FURUHASHI et al by the texture mip mapping teaching of SCHILLING et al because both inventions share similar functions of texture mapping. Further, SCHILLING et al provides the following advantage - "..the present invention provides a data compression system to reduce memory storage and bandwidth requirements in a simple, yet fast manner, and to therefore reduce system costs" (column 2, lines 18-22).

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. MIGDAL et al US Patent Number 5,760,783. CHAUVIN et al US Patent Number 6,008,820. FUJIMURA et al US Patent Number 6,411,303. FURUHASHI et al US Patent Number 6,011,564. REDMANN et al US Patent Number 5,696,892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Blackman FRIDAY from 8 a.m. to 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi, can be reached on (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry) Or:

(703) 746-5731 (for informal or draft communications sent directly to examiner's PC, please label "PROPOSED" or "DRAFT",)

Hand-delivered responses should be brought to Crystal Park 11, 2121 Crystal Drive, Arlington. VA.,

Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Art Unit: 2672

Anthony J. Blackman

Patent Examiner

9/10/2002

JEFFERY BRIER
PRIMARY EXAMINER